



Docket No.: A0312.70410US00  
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Stephen J. Plante et al.  
Serial No.: 09/923,225  
Confirmation No.: 8975  
Filed: August 6, 2001  
For: HIGH PERFORMANCE TURBO AND VITERBI CHANNEL  
DECODING IN DIGITAL SIGNAL PROCESSORS  
Examiner: J. D. Torres  
Art Unit: ~~2133~~ 2112

<b>Certificate of Mailing Under 37 CFR 1.8(a)</b>	
I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as First Class Mail, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.	
Dated: <del>February</del> 2008 March 6, 2008	<i>Paula K. Fairweather</i> Paula K. Fairweather

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

**DECLARATION OF STEPHEN J. PLANTE UNDER 37 C.F.R. §1.131**

I, STEPHEN J. PLANTE, state and declare the following:

1. I am an inventor on the above-identified patent application.
2. Prior to June 21, 2001, Applicants for the above-identified patent application had conceived and reduced to practice the invention of each of claims 1-6, 18, 25 and 26, as presently amended, in the above-identified patent application.
3. Attached hereto as Exhibit A is a true copy, with personal information of the inventors and confidentiality notices redacted, of an invention disclosure document which describes the subject matter of, and was used to prepare, the above-identified patent application.

This document is signed by me and is dated April 7, 2000. The invention disclosure document includes an Invention Disclosure form of three (3) pages and five (5) attachments, which, for convenience, have been identified as Attachments AA-EE.

4. As Exhibit A shows, the invention of claims 1-6, 18, 25 and 26 in the above-identified patent application was reduced to practice prior to June 21, 2001. The claimed invention is disclosed throughout Exhibit A. However, the following passages are specifically noted. The trellis function and the add, compare, select (ACS) instruction are described at pages 2-5 and 9-12 of Attachment AA. The ACS instruction described in Exhibit A corresponds to the trellis instruction recited in the claims of the subject application. Implementation of the ACS instruction is disclosed at pages 17 and 18 of Attachment AA. Fig. 9 of the subject application corresponds to the figure on page 9 of Attachment AA. Fig. 10 of the subject application corresponds to the figure on page 11 of Attachment AA. Fig. 18 of the subject application corresponds to the figure on page 17 of Attachment AA.

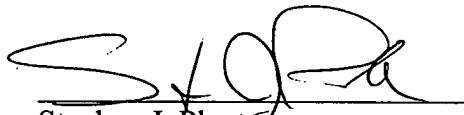
Improvements to the performance of the TigerSHARC digital signal processor (DSP) provided by three instructions, including the ACS instruction, are disclosed at pages 1-2 and 7-8 of Attachment BB and at pages 1-2 of Attachment DD.

The ACS instruction and a code sequence using the ACS instruction are disclosed at pages 20 and 22 of Attachment EE. A block diagram of the TigerSHARC DSP for implementing the ACS instruction is disclosed at page 29 of Attachment EE. Fig. 11 of the present application corresponds to the code sequence shown on page 22 of Attachment EE. Fig. 7 of the present application corresponds generally to the DSP block diagram shown on page 29 of Attachment EE.

5. There was no significant development of the claimed invention after June 21, 2001. The claimed method and processor using the ACS instruction were reduced to practice and included in the design for the TigerSHARC digital signal processor product before June 21, 2001.

6. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

3/3/08  
Date

  
Stephen J. Plante